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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE  
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ROOSEVELT ROAD, SECTION 2  
TAIPEI, 100  
TAIWAN

EXAMINER
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PIZIALI, JEFFREY J

ART UNIT	PAPER NUMBER
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2629

NOTIFICATION DATE	DELIVERY MODE
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06/17/2008

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/708,365		HUNG ET AL.	
	<b>Examiner</b>		<b>Art Unit</b>	
	Jeff Piziali		2629	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period **will** apply and **will** expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply **will**, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 February 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,2 and 4-19 is/are pending in the application.
- 4a) Of the above claim(s) 1,2 and 4-8 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 9-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 February 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### *Election/Restrictions*

1. Applicants' election of Species II (i.e., Claims 9-19) in the reply filed on 6 February 2007 is acknowledged. Because applicants did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).
2. Claims 1, 2, and 4-8 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 6 February 2007.
3. Applicants are reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

### *Drawings*

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: "**110**" (see Fig. 1a). Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the

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specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. The drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicants' cooperation is requested in correcting any errors of which applicants may become aware in the figures.

### *Specification*

6. The disclosure is objected to because of the following informalities:

The phrase, "***In conventional art, Gamma voltages are generated externally in replace of the embedded Gamma circuit of driving IC***" should be corrected, for example to, "***In the conventional art, Gamma voltages are generated externally in the place of the embedded Gamma circuit of a driving IC***" (see Paragraph 8, Lines 1-3).

Appropriate correction is required.

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7. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicants' cooperation is requested in correcting any errors of which applicants may become aware in the specification.

***Claim Rejections - 35 USC § 112***

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 9-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter, ***"the first terminal of any one of the Gamma resistors receiving one bit signal in digital form of a Gamma setup signal comprising a plurality of bit signals"*** (in line 4). It would be unclear to one having ordinary skill in the art whether the ***"any one of the Gamma resistors"*** receives ***"one bit signal"***; or rather whether ***"any one of the Gamma resistors"*** receives ***"a plurality of bit signals"***.

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11. Claim 9 recites the limitation "**current output**" in line 7. There is insufficient antecedent basis for this limitation in the claim.

12. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter, "**a feedback resistor, having a third terminal and a fourth terminal**" (in line 3). It would be unclear to one having ordinary skill in the art whether the "**feedback resistor**" has two terminals; or rather whether the "**feedback resistor**" has four terminals.

An omitted structural cooperative relationship results from the claimed subject matter, "**is coupled**" (in line 6). It would be unclear to one having ordinary skill in the art what the subject of "**is coupled**" is intended to be. The feedback resistor? The third terminal? The second input terminal? Etc?

An omitted structural cooperative relationship results from the claimed subject matter, "**which are coupled**" (in line 7). It would be unclear to one having ordinary skill in the art what the subject of "**which are coupled**" is intended to be. The Gamma resistors? The second terminal? The feedback resistor? The third terminal? The second input terminal? Etc?

An omitted structural cooperative relationship results from the claimed subject matter, "**others**" (in line 10). It would be unclear to one having ordinary skill in the art what the subject of "**others**" is intended to refer to. Other resistances? Other Gamma resistors? The second terminal? The feedback resistor? The third terminal? The second input terminal? Etc?

13. Claim 10 recites the limitations: "*the amount*" (in line 8) and "*the amount*" (in line 9).

There is insufficient antecedent basis for these limitations in the claim.

14. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter, "*comprises*" (in line 4). It would be unclear to one having ordinary skill in the art what the subject of "*comprises*" is intended to be. The digital form? Each of the Gamma setup signals? The plurality of Gamma setup signals? The control/modify circuit? Etc?

An omitted structural cooperative relationship results from the claimed subject matter, "*outputting*" (in line 8). It would be unclear to one having ordinary skill in the art what the subject of "*outputting*" is intended to be. The plurality of Gamma setup signals? The programmable Gamma circuit? The driving circuit? The display panel? The control/modify circuit? Etc?

An omitted structural cooperative relationship results from the claimed subject matter, "*correspondingly according*" (in line 9). It would be unclear to one having ordinary skill in the art what the subject of "*correspondingly according*" is intended to mean. As such, it would be unclear to an artisan what the relationship is intended to be between the "*Gamma voltage signals*" and the "*Gamma setup signals*."

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15. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter, "*correspondingly according*" (in line 4). It would be unclear to one having ordinary skill in the art what the subject of "*correspondingly according*" is intended to mean. As such, it would be unclear to an artisan what the relationship is intended to be between the "*Gamma voltage signals*" and the "*Gamma setup signals*."

An omitted structural cooperative relationship results from the claimed subject matter, "*the Gamma setup signals that is received*" (in line 4). It would be unclear to one having ordinary skill in the art whether plural "*Gamma setup signals*" are received; or rather whether a single "*Gamma setup signal*" is received.

16. Claim 16 recites the limitations: "*the Gamma setup signal*" (in line 5); "*current outputted*" (in line 6); "*the amount*" (in line 7); and "*the amount*" (in line 8). There is insufficient antecedent basis for these limitations in the claim.

17. Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter, "*each of the Gamma resistors is coupled together*" (in line 3). It would be unclear to one having



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ordinary skill in the art whether a plurality of "***Gamma resistors***" are coupled to each other; or rather whether a single "***Gamma resistor***" is coupled to some other claimed element.

An omitted structural cooperative relationship results from the claimed subject matter, "***others***" (in line 9). It would be unclear to one having ordinary skill in the art what the subject of "***others***" is intended to refer to.

18. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter, "***a feedback resistor, having a third terminal and a fourth terminal***" (in line 3). It would be unclear to one having ordinary skill in the art whether the "***feedback resistor***" has two terminals; or rather whether the "***feedback resistor***" has four terminals.

An omitted structural cooperative relationship results from the claimed subject matter, "***a first terminal, a second terminal***" (in claim 17, line 4). It would be unclear to one having ordinary skill in the art whether these claimed "***a first terminal, a second terminal***" are identical to the earlier claimed "***a first terminal and a second terminal***" (in claim 16, line 4); or rather whether "***a first terminal, a second terminal***" are different and distinct from the earlier claimed "***a first terminal and a second terminal***".

An omitted structural cooperative relationship results from the claimed subject matter, "***is coupled***" (in line 6). It would be unclear to one having ordinary skill in the art what the subject of "***is coupled***" is intended to be.

An omitted structural cooperative relationship results from the claimed subject matter, "***which are coupled***" (in line 7). It would be unclear to one having ordinary skill in the art what the subject of "***which are coupled***" is intended to be.

19. The remaining claims are rejected under 35 U.S.C. 112, second paragraph, as being dependent upon rejected base claims.

***Claim Rejections - 35 USC § 102***

20. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

21. Claims 9-19 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Medina et al (US 6,359,389 B1)***.

Regarding claim 9, Medina discloses a programmable Gamma circuit [e.g., Figs. 3 & 6; 240b], comprising:

a plurality of Gamma resistors [e.g., Fig. 5; 514 & 524] in parallel (wherein the resistors are all illustrated as being vertically aligned in a parallel plane),

each of the Gamma resistors having a first terminal and a second terminal (see the entire document, including Column 8, Line 65 - Column 9, Line 22),

the first terminal of any one of the Gamma resistors receiving one bit signal in digital form of a Gamma setup signal [e.g., Fig. 6; 410] comprising a plurality of bit signals, and

the second terminal of each of the Gamma resistors being coupled together where current outputted from each of the Gamma resistors is summed up to a Gamma current (see the entire document, including Column 9, Line 50 - Column 10, Line 21); and

an amplifying unit [e.g., Fig. 6; 520 + R], receiving the Gamma current and outputting a Gamma voltage signal [e.g., Fig. 6;  $V_{OUT}$ ] correspondingly (see the entire document, including Column 9, Lines 23-48).

Regarding claim 10, Medina discloses the amplifying unit comprises:

a feedback resistor [e.g., Fig. 6; R], having a third terminal and a fourth terminal; and

an operational amplifier [e.g., Fig. 6; 520], having a first input terminal, a second input terminal and an output terminal,

wherein the first input terminal is coupled to a voltage level [e.g., Fig. 6; "ground"],

the second input terminal is coupled to the third terminal of the feedback resistor and is coupled to the second terminal of each of the gamma resistors, which are coupled together, to receive the Gamma current,

the amount of the bit signals being equal to the amount of the Gamma resistors, each of the Gamma resistors comprising a resistance different from the others, and

the output terminal and the fourth terminal of the feedback resistor are coupled and output the Gamma voltage signal (see the entire document, including Column 9, Lines 23-48).

Regarding claim 11, Medina discloses the voltage level is ground voltage level (see the entire document, including Column 9, Lines 34-40).

Regarding claim 12, Medina discloses the programmable Gamma circuit is applied to a driving circuit of a display apparatus [e.g., Fig. 3; 280] (see the entire document, including Column 7, Lines 12-15).

Regarding claim 13, Medina discloses the display apparatus is a liquid crystal display (see the entire document, including Column 5, Lines 11-32).

Regarding claim 14, this claim is rejected by the reasoning applied in rejecting claims 9 and 12; furthermore, Medina discloses a display apparatus (see the entire document, including Column 5, Lines 11-32), comprising:

a display panel [e.g., Fig. 3; 280] (see the entire document, including Column 7, Lines 12-15);

a control/modify circuit [e.g., Fig. 3; 250], for outputting a plurality of Gamma setup signals [e.g., Fig. 6; 410],

wherein each of the Gamma setup signals is in digital form and comprises a plurality of bit signals; and

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a driving circuit [e.g., Fig. 3; 240b + 260 + 270] (see the entire document, including Column 8, Line 65 - Column 9, Line 22), coupling to the control/modify circuit and the display panel,

wherein the driving circuit comprises a programmable Gamma circuit [e.g., Figs. 3 & 6; 240b] (see the entire document, including Column 9, Line 50 - Column 10, Line 21),

the programmable Gamma circuit receiving the plurality of Gamma setup signals, and outputting a plurality of Gamma voltage signals [e.g., Fig. 6;  $V_{OUT}$ ] correspondingly according to the Gamma setup signals (see the entire document, including Column 9, Lines 23-48).

Regarding claim 15, this claim is rejected by the reasoning applied in rejecting claim 9.

Regarding claim 16, this claim is rejected by the reasoning applied in rejecting claims 9 and 10.

Regarding claim 17, this claim is rejected by the reasoning applied in rejecting claim 10.

Regarding claim 18, this claim is rejected by the reasoning applied in rejecting claim 11.

Regarding claim 19, this claim is rejected by the reasoning applied in rejecting claim 13.

22. Claims 9, 12-16, and 19 are rejected under 35 U.S.C. 102(e) as anticipated by

***Mametsuka (US 7,030,840 B2).***

Regarding claim 9; Mametsuka discloses a programmable Gamma circuit [e.g., Fig. 3; 3, 31], comprising:

a plurality of Gamma resistors [e.g., Fig. 3; VR\_R, VR\_G, VR\_B] in parallel,  
each of the Gamma resistors having a first terminal [e.g., Fig. 3; connected to VSS] and a second terminal [e.g., Fig. 3; connected to R9],

the first terminal of any one of the Gamma resistors receiving one bit signal [e.g., Fig. 3; VSS or OFF] in digital form of a Gamma setup signal comprising a plurality of bit signals (see the entire document, including Figs. 3 & 4; wherein  $\gamma\text{SEL}1$ ,  $\gamma\text{SEL}2$ , and  $\gamma\text{SEL}3$  digitally [e.g., on/off] determine whether or not VSS is provided individually to the Gamma resistors), and

the second terminal of each of the Gamma resistors being coupled together where current outputted from each of the Gamma resistors is summed up to a Gamma current [e.g., Fig. 3; VREF] (see the entire document, including Column 5, Line 53 - Column 6, Line 7); and

an amplifying unit [e.g., Fig. 2; 6, 23], receiving the Gamma current and outputting a Gamma voltage signal [e.g., Fig. 2; OUT1-OUTn/3] correspondingly (see the entire document, including Column 4, Line 36 - Column 5, Line 52).

Regarding claim 12, Mametsuka discloses the programmable Gamma circuit is applied to a driving circuit [e.g., Fig. 2; 23] of a display apparatus [e.g., Fig. 2; 10] (see the entire document, including Column 4, Line 36 - Column 5, Line 52).

Regarding claim 13, Mametsuka discloses the display apparatus is a liquid crystal display (see the entire document, including Column 9, Lines 24-32).

Regarding claim 14, Mametsuka discloses a display apparatus (see the entire document, including Column 9, Lines 24-32), comprising:

- a display panel [e.g., Fig. 2; 10];

- a control/modify circuit [e.g., Fig. 3;  $\gamma$ SEL1,  $\gamma$ SEL2, and  $\gamma$ SEL3 controlling  $\gamma$ SW\_R,  $\gamma$ SW\_G, and  $\gamma$ SW\_B], for outputting a plurality of Gamma setup signals [e.g., Fig. 3; signals sent via  $\gamma$ SEL1,  $\gamma$ SEL2, and  $\gamma$ SEL3],

- wherein each of the Gamma setup signals is in digital form and comprises a plurality of bit signals (see the entire document, including Figs. 3 & 4; wherein  $\gamma$ SEL1,  $\gamma$ SEL2, and  $\gamma$ SEL3 digitally [e.g., on/off] determine whether or not VSS is provided individually to the Gamma resistors); and

- a driving circuit [e.g., Fig. 2; 6, 23], coupling to the control/modify circuit and the display panel (see the entire document, including Column 4, Line 36 - Column 5, Line 52),

- wherein the driving circuit comprises a programmable Gamma circuit [e.g., Fig. 3; 3, 31],

- the programmable Gamma circuit receiving the plurality of Gamma setup signals, and outputting a plurality of Gamma voltage signals [e.g., Fig. 3; VREF] correspondingly according to the Gamma setup signals (see the entire document, including Column 5, Line 53 - Column 6, Line 7).

Regarding claim 15, this claim is rejected by the reasoning applied in rejecting claim 9.

Regarding claim 16, this claim is rejected by the reasoning applied in rejecting claim 9.

Regarding claim 19, this claim is rejected by the reasoning applied in rejecting claim 13.

***Claim Rejections - 35 USC § 103***

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

24. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

25. Claims 9-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Medina et al (US 6,359,389 B1)* in view of *Mametsuka (US 7,030,840 B2)*.



Regarding claims 9-19; as detailed above, Medina discloses the instantly claimed invention in full.

However, should it be shown that Medina neglects teaching a plurality of Gamma resistors in parallel, in combination with the remaining limitations of the instantly claimed invention; Mametsuka discloses a plurality of Gamma resistors [e.g., Fig. 3; VR\_R, VR\_G, VR\_B] in parallel, wherein the second terminal of each of the Gamma resistors is coupled together (see the entire document, including Column 5, Line 53 - Column 6, Line 7).

Medina and Mametsuka are analogous art, because they are from the shared inventive field of adjustable gamma correction circuits for display devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use Mametsuka's reference gradation voltage generating circuit [e.g., Mametsuka: Fig. 3; 3] as Medina's reference gradation voltage generating circuit(s) [e.g., Medina: Fig. 6; R0-R16 & 550(0)-550(16) and/or Fig. 5; 512, 514, 516, 522, 524, & 526], so as to provide a display device in which a complicated circuit configuration is not required in compensating for differences in the luminosity characteristics of pixels, so that a color image can be uniformly displayed without increasing the number of circuit components (see the entire document, including Mametsuka: Column 2, Lines 1-5), arriving at the instant invention as presently claimed.

26. Claims 9-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Mametsuka* (US 7,030,840 B2) in view of *Medina et al* (US 6,359,389 B1).

Regarding claims 9, 12-16, and 19; as detailed above, Mametsuka discloses the instantly claimed invention in full.

However, should it be shown that Mametsuka neglects teaching an amplification unit, in combination with the remaining limitations of the instantly claimed invention; Medina discloses an amplification unit [e.g., Fig. 6; 520 + R], receiving the Gamma current and outputting a Gamma voltage signal [e.g., Fig. 6;  $V_{OUT}$ ] correspondingly (see the entire document, including Column 9, Lines 23-48).

Mametsuka and Medina are analogous art, because they are from the shared inventive field of adjustable gamma correction circuits for display devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use Medina's amplification unit(s) [e.g., Medina: Fig. 6; 520 + R] with Mametsuka's programmable Gamma circuit [e.g., Mametsuka: Fig. 3; 3, 31], so as to provide a display device that has an adjustable gamma response without an incidental degradation of gray scale resolution (see the entire document, including Medina: Column 3, Lines 8-11), arriving at the instant invention as presently claimed.

Regarding claim 10, Medina discloses the amplifying unit comprises:  
a feedback resistor [e.g., Fig. 6; R], having a third terminal and a fourth terminal; and  
an operational amplifier [e.g., Fig. 6; 520], having a first input terminal, a second input terminal and an output terminal,  
wherein the first input terminal is coupled to a voltage level [e.g., Fig. 6; "ground"],

the second input terminal is coupled to the third terminal of the feedback resistor and is coupled to the second terminal of each of the gamma resistors, which are coupled together, to receive the Gamma current,

the amount of the bit signals being equal to the amount of the Gamma resistors, each of the Gamma resistors comprising a resistance different from the others, and

the output terminal and the fourth terminal of the feedback resistor are coupled and output the Gamma voltage signal (see the entire document, including Column 9, Lines 23-48).

Regarding claim 11, Medina discloses the voltage level is ground voltage level (see the entire document, including Column 9, Lines 34-40).

Regarding claim 17, this claim is rejected by the reasoning applied in rejecting claim 10.

Regarding claim 18, this claim is rejected by the reasoning applied in rejecting claim 11.

### ***Response to Arguments***

27. Applicant's arguments filed 25 February 2008 have been fully considered but they are not persuasive.

The Applicant contends, "*Medina et al. fails to teach or suggest 'a plurality of Gamma resistors communicated in parallel' and 'the second terminal of each of the Gamma resistors*

*being coupled together' as recited in amended claim 9"* (see Page 11, Paragraph 2 of the Amendment filed 25 February 2008). However, the examiner respectfully disagrees.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "*a plurality of Gamma resistors communicated in parallel*") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Medina discloses a plurality of Gamma resistors [e.g., Fig. 5; 514 & 524] in parallel (*wherein the resistors are all illustrated as being vertically aligned in a parallel plane*), each of the Gamma resistors having a first terminal [e.g., top] and a second terminal [e.g., bottom] (see the entire document, including Column 8, Line 65 - Column 9, Line 22), and the second terminal of each of the Gamma resistors being coupled together (see the entire document, including Fig. 5; Column 9, Line 50 - Column 10, Line 21 -- *wherein the second, lower terminal of each Gamma resistor is commonly coupled together at ground*).

The Applicant contends, "*Medina et al. fails to teach or suggest 'the amount of the bit signals being equal to the amount of the Gamma resistors' and 'each of the Gamma resistors having a resistance different from others' as recited in amended claim 10. Therefore, dependent claim 10 patently defines over the prior art reference, and should be allowed*" (see the entire

document, including Page 12, Paragraph 2 of the Amendment filed 25 February 2008). However, the examiner respectfully disagrees.

Medina discloses the first terminal of any one of the Gamma resistors [e.g., Fig. 5; 514 & 524] receiving one bit signal in digital form of a Gamma setup signal [e.g., Fig. 6; 410] comprising a plurality of bit signals, wherein the amount of the bit signals being equal to the amount of the Gamma resistors, each of the Gamma resistors comprising a resistance different from the others (see the entire document, including Fig. 5; Column 9, Line 50 - Column 10, Line 21).

Medina explains, "*Circuit 510(0) generates a voltage E1 which is coupled through a resistor to the inverting terminal of buffer (operational amplifier) 520(0). Circuit 510(0) also generates a voltage E2 which is coupled through a resistor to the non-inverting terminal of buffer 520(0) which is also coupled to node 535(0). The non-inverting terminal is coupled through a resistor to the output of the buffer 520(0) which supplies the output reference voltage (Vout0) for this stage. It is appreciated that programming line 410(0) is coupled to controller 250 to allow programming of the voltage values E1 and E2.*

*"The output voltage, Vout0, can be expressed according to the following relationship:*

$$V_{out0} = V_{ref0} + E2 - E1$$

*"wherein E2 and E1 correspond to circuit 510(0). It is appreciated that any of the discrete reference voltages, Vouti, can be expressed according to:*

$$V_{outi} = V_{refi} + E2 - E1$$

*"wherein E2 and E1 correspond to circuit 510(i).*

*"Resistor R1550(1) is coupled in series to resistor R0 and resistor R1 is also coupled to an analogous stage circuit containing circuit 510(1), buffer 530(1), circuit 510(1), and buffer 520(1). **The output reference voltage,  $V_{out}(1)$ , is controlled by program line 410(1).** The above circuit is replicated for each state of the ALC 240b. For instance, resistor R1550(15) is coupled in series to resistor R16 and resistor R15 is also coupled to an analogous stage circuit containing circuit 510(15), buffer 530(15), circuit 510(15), and buffer 520(15). **The output reference voltage,  $V_{out}(15)$ , is controlled by program line 410(15).** Resistor 16 is coupled to ground, or to a low voltage source. The discrete reference voltages,  $V_{out}(0)$ - $V_{out}(15)$  of ALC 240b are programmed by controller 250 via lines 410(0)-410(15). As stated above, by controlling the values of the discrete reference voltages generated by ALC 240b, the controller 250 can alter the gamma response (or profile) of the display screen without reducing its gray scale resolution or color depth" (see the entire document, including Column 9, Line 38 - Column 10, Line 10).*

As such, Medina teaches the amount of the bit signals being equal to the amount of the Gamma resistors. Each output reference voltage,  $V_{out}(i)$ , is controlled by program line 410(i). Wherein each program line 410(i) programs the voltage values E1 and E2, by setting the amount of the Gamma resistors.

Medina explains, "*It is appreciated that programmable potentiometers 514 and 524 can be controlled by a control line (not shown in FIG. 5) from the controller device 250*" (see the entire document, including Column 9, Lines 19-22).

Furthermore, each of Medina's Gamma resistors [e.g., Fig. 5; 514 & 524] has a resistance different from others. Each circuit [e.g., Figs. 5 & 6; 510(i)] outputs two different voltage values [e.g., Figs. 5 & 6; E1 and E2].

Clearly the two voltage values [e.g., Figs. 5 & 6; E1 and E2] are different -- otherwise there would be no point to generating both voltage values [e.g., Figs. 5 & 6; E1 and E2]. If the two voltage values [e.g., Figs. 5 & 6; E1 and E2] were the same, there would be no point to generating them both with two separate sets of circuits (as illustrated in Medina's Figure 5).

Each output reference voltage,  $V_{out}(i)$  is controlled by the relationship " $V_{out}(i) = V_{ref}(i) + E2 - E1$ ". If the two voltage values [e.g., Figs. 5 & 6; E1 and E2] were the same,  $V_{out}(i)$  would instead be controlled by the relationship " $V_{out}(i) = V_{ref}(i)$ ." and there would be no point to generating either of the two voltage values [e.g., Figs. 5 & 6; E1 and E2].

In order for the two voltage values [e.g., Figs. 5 & 6; E1 and E2] to be different, each of Medina's Gamma resistors [e.g., Fig. 5; 514 & 524] must inherently have a resistance different from others.

The Applicant contends, "*Claim 14 is similar to claim 9, for the above reasons, claim 14 is patentable over Medina et al.*" (see Page 12, Paragraph 4 of the Amendment filed 25 February 2008). However, the examiner respectfully disagrees.

Independent claim 14 lacks the Applicant's argued subject matter of "*a plurality of Gamma resistors communicated in parallel*" and "*the second terminal of each of the Gamma resistors being coupled together*" as newly recited in amended independent claim 9.

Applicant's arguments with respect to claims 9-19 have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

### ***Conclusion***

28. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. The documents listed on the attached '*Notice of References Cited*' are cited to further evidence the state of the art pertaining to programmable Gamma circuits.



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29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Wherein independent claim 9 was amended substantially in scope. Furthermore, independent claim 14 changed "the Gamma setup signals" to "the plurality of Gamma setup signals" (see line 8) -- unexpectedly and newly limiting the programmable Gamma circuit to receiving all (as opposed to merely some) of "the plurality of Gamma setup signals" as amended. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/  
Primary Examiner, Art Unit 2629  
29 May 2008